

Appl. No. 09/683,647  
Amdt. dated July 27, 2005  
Reply to Office action of June 15, 2005

**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application:

**Listing of Claims:**

- 1 (original): A data transmission circuit for transmitting data comprising:
- 5       an internal circuit for providing data;  
      a register electrically connected to the internal circuit for temporarily storing the  
          data transmitted from the internal circuit; and  
      a control circuit for controlling operations of the internal circuit and  
          the register;
- 10       wherein if data inputted to the register is a specific data, the internal  
      circuit will repeatedly output the specific data to the register so as to  
      prolong transmission time of the specific data.
- 2 (original): The data transmission circuit of claim 1 further comprising an
- 15       output circuit electrically connected to the register for outputting the  
      data transmitted from the register.
- 3 (original): The data transmission circuit of claim 2 wherein the register
- 20       comprises a D flip-flop for outputting data transmitted from the  
      internal circuit to the output circuit and feeding back the data to the  
      internal circuit.
- 4 (currently amended): The data transmission circuit of claim 2 wherein
- 25       when the ~~input~~ internal circuit repeatedly outputs the specific data to the  
      register, the register will prolong the time that the specific data is  
      outputted to the output circuit, and when the register prolongs the time  
      that the specific data outputted to the output circuit, the control circuit  
      will output a control signal to terminate the register from outputting

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the specific data to the output circuit.

- 5 (currently amended): The data transmission circuit of claim 1 wherein the  
input internal circuit comprises a multiplexer, the multiplexer  
5 comprising:  
a first input end electrically connected to an output end of the register  
for inputting data outputted by the register;  
a second input end for inputting data to be transmitted by the data  
transmission circuit; and  
10 a selecting end electrically connected to the control circuit for  
receiving a selecting signal transmitted from the control circuit.
- 6 (currently amended): The data transmission circuit of claim 5 wherein  
when the second input end receives the specific data and the  
15 multiplexer has transmitted the specific data to the register, the control  
circuit will ~~using~~ transmit the selecting signal to the control end so  
that the multiplexer will continue to output the specific data to the  
register.
- 20 7 (original): The data transmission circuit of claim 5 wherein the specific  
data is a last data packet within a plurality of data packets successively  
inputted to the second input end.
- 8 (original): The data transmission circuit of claim 1 being formed on a  
25 north bridge chip of a motherboard.
- 9 (currently amended): A data transmission method of a data transmission circuit, the  
data transmission circuit comprising:  
an internal circuit for providing data; and

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a register electrically connected to the ~~input~~ internal circuit for temporarily storing data transmitted from the ~~input~~ internal circuit; and  
a control circuit for controlling operations of the internal circuit and the register;

5 the method comprising:

when data inputted to the ~~input circuit being~~ register by the internal circuit is specific data, the specific data ~~will be~~ being repeatedly transmitted to the register to prolong transmission time of the specific data.

10 10 (currently amended): The data transmission method of claim 9 further comprising:

for ~~prolonged~~ prolonging transmission time of the specific data, ~~on the~~ control circuit transmitting a control signal ~~will be transmitted~~ to terminate transmission of the specific data.

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11 (currently amended): The data transmission method of claim 9 wherein the specific data being a last data packet of a plurality of data packets gets successively inputted to the ~~input circuit~~ register.

20 12 (currently amended): The data transmission method of claim 9 wherein the data transmission circuit ~~being~~ is located on a north bridge of a motherboard.